**Dr. MADHUSUDAN GHOSH**

**Designation:** Associate Professor of Physics

**About Me:** Dr. Ghosh received B.Sc. (Physics), M.Sc. (Physics) and Ph.D. (Science) degree from Burdwan University, West Bengal, India in the year 1997, 1999 and 2013 respectively. At present he hold a faculty positions at the department of Physics, Maulana Azad College, Kolkata-700013, West Bengal, India. His research interest centers on field of synchronous communication system (PLL based) and nonlinear dynamics of discrete controlled system. He has published about 9 research papers in inland and foreign journals and has contributed about 3 technical papers in national and international seminars and conferences.

**Experience / Expertise:**
Dr. Ghosh presently working as Associate Professor of Physics to teach in UG level (Hons/General) since 2002 and still continuing

**Qualifications:**
- Dr. Ghosh received Ph.D.(Science) degree from Burdwan University, West Bengal, India in the year 2013
  Title of PhD thesis: STUDIES ON JITTER RESPONSE AND DESIGN-DEPENDENT DYNAMICS OF SOME PLL-BASED CLOCK/DATA RECOVERY CIRCUITS

**Specialisation & Area of Interests:**
- Dr. Ghosh's specialisation in M.Sc. degree is "Radiophysics & Electronics". His areas of interest are Communication Electronics, Non-linear dynamics & Chaos, Electricity etc.

**Current Teaching:**
- Dr. Ghosh served three different Government Colleges (A.B.N. Seal College, Krishnagore Govt. College & Maulana Azad College) and taught different topics of Physics (Hons and General) syllabus under different Universities. Presently he has been teaching Electronics, Static Electricity, Relativity etc.

**Research Interests:**
His research interest centers on field of synchronous communication system and nonlinear dynamics of discrete controlled systems
Main Research Projects – Dr. Ghosh completed the UGC sponsored minor research project (MRP) for two years with effect from April, 2014 and UGC sanction letter no.-PSW-058/13-14 dated 18th March, 2014 and approved amount for the said project was Rs.4.5 Lakh.
Title of the Project: **JITTER REDUCTION AND DESIGN DEPENDENT DYNAMICS OF CARRIER/CLOCK RECOVERY CIRCUITS**

**Selected Publications:**
**A) Journal Publications:**

(i) **M. Ghosh**, Dr A. Hati, Dr B. C. Sarkar, "*phase detector for data clock recover circuit*", Institute of Electrical Engineers, UK (2002), Vol: 38, No.: 04, pp: 161-163, 14th February, 2002

(ii) **M. Ghosh**, Dr A. Hati, Dr B. C. Sarkar, "*On improving the spectral purity of the regenerated clock signal in a data clock recovery circuit*", Indian Journal of Engineering and Material Science (IJEMS), Vol: 09, pp: 255-259, August, 2002

(iii) **M. Ghosh**, T. Banerjee and B. C. Sarkar , "*Design limitations and its effect in the performance of ZC1-DPLL*", ACEEE International Journal on Communication, Vol: 3, Issue: 1, pp: 48-52, 2012

(iv) **M. Ghosh**, T. Banerjee and B. C. Sarkar , "*Nonlinear Dynamics and Chaos in Second Order ZC1-DPLLs with Inherent Time Delay*", International Journal of Engineering and Advanced Technology (IJEAT), Vol: 01, no.-6, pp: 235-242, Aug, 2012

(v) **M Ghosh,** "*Performance Enhancement of Digital Phase Locked Loop (DPLL) Based FM Demodulator by Using of Variable Gain Control in the Negative Region of the Input Signal*", MAC Journal of Basic and Applied Sciences, Volume 2, No. 1, pp - 67-74, March 2015

(vi) **M Ghosh**, S. Dutta, "*A Fast Acquisition Data Clock Recovery Circuit*", MAC Journal of Basic and Applied Sciences, Volume 2, No. 1, pp - 111-116, March 2015

(vii) **M. Ghosh,** "*Improvement of the Performance of DPLL Based FM Demodulator by using of Variable Gain Control in the Positive Region of the Input Signal*", International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), Volume 4, Issue 5, pp - 1359-1362, May 2015

(viii) **M. Ghosh,** "*Additive Noise Response of Some Novel Phase Detector Based Charge Pump PLL Circuits; an Analytical and Simulation*", Indian Journal of Applied Research (IJAR), Volume 5, Issue 10, pp - 726-731, October 2015, ISSN No: 2249-555X

(ix) **M. Ghosh,** "*Nonlinear Dynamics and Chaotic Behavior of Delayed Digital Phase Locked Loop*", Scientific Voyage, Volume 1, Issue 3, pp: 7-14, October 2015 ISSN No: 2395-5546

**B) Proceedings:**

(i) **M. Ghosh,** "*Dividerless frequency synthesizer using a new phase detector*", Proceedings of E.P. Centenary Seminar organized jointly by the younger member section, Calcutta branch of the institute of Electrical Engineers and the IEE students centre, Institute of Radio physics and Electronics, University of Calcutta, India, on 21st day of August, 2002 at the institute of radio physics and Electronics, University of Calcutta, India.

(ii) **M. Ghosh**, T. Banerjee and B. C. Sarkar , "*Nonlinear Dynamics of DPLL With Inherent Time Delay*", Proceedings of National Conference on Nonlinear Systems &Dynamics, Saha Institute of Nuclear Physics, Kolkata, India, March 5-7, 2009.

(iii) **M. Ghosh** , "*Effect of sampling pulse width in the performance of DPLL based FM demodulator and its modification*", Proceedings of National Workshop on "Quantum Perspective of Advance Materials (QPAM-11)" organized by Department of Physics and Technophysics, Vidyasagar University from March 23-25, 2011.

- ***Posters: 01 (One)***

(i) Presented a research paper entitled "*Effect of sampling pulse width in the performance of DPLL based FM demodulator and its modification*" in the National Workshop on "Quantum Perspective of Advance Materials (QPAM-11)" organized by Department of Physics and Technophysics, Vidyasagar University from March 23-25, 2011.

- ***Conference Talks: 01 (One)***

(i) Presented a research paper entitled "*Dividerless frequency synthesizer using a new phase detector*" in the E.P. Centenary Seminar organized jointly by the younger member section, Calcutta branch of the institute of Electrical Engineers and the IEE students centre, Institute of Radio physics and Electronics, University of Calcutta, India, on 21st day of August, 2002 at the institute of radio physics and Electronics, University of Calcutta, India.

**Contact Details:**

Email: madhu_sg2000@yahoo.com
Telephone number(s): 9432989926
Postal Address: ROYAL PLAZA, 174 G.B. Road, Nagerbazar, Dum Dum, Kolkata-700028

**Other Information:**

**1)** Dr. Ghosh has been working as Reviewer of International Journal of Electronics, UK

**2) Project Work:**

(i) Perform DBT sponsored project work entitled "**A Fast Acquisition Data Clock Recovery Circuit**" in December, 2013

(ii) Performing a UGC sponsored minor research project (MRP) for two years with effect from April, 2014 and UGC sanction letter no.-PSW-058/13-14 dated 18th March, 2014.

Title of the Project: **JITTER REDUCTION AND DESIGN DEPENDENT DYNAMICS OF CARRIER/CLOCK**

(iii) Perform DBT sponsored project work entitled "**Variable voltage source using weighted resistor digital to analog (D/A) converter**" from 26/02/2015 to 28/02/2015.